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synchronize execution dummy code

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[Preferences](#)**Web** Results 1 - 10 of about 175,000 for synchronize execution dummy code. (0.26 seconds)ISDN multimedia communications system - US Patent 5206859

Program **execution** starts with initialization step 50 in which a video-mode flag ... At the distant station, the **dummy code** is separated by **sync** separator 5. ...

[www.patentstorm.us/patents/5206859-description.html](http://www.patentstorm.us/patents/5206859-description.html) - 33k -

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Processing instructions up to load instruction after executing ...

an instruction **execution** controller for executing instructions subsequent to ..... and for this reason this decoder 1011 outputs a **dummy code** which does not ...

[www.freepatentsonline.com/5968135.html](http://www.freepatentsonline.com/5968135.html) - 67k - [Cached](#) - [Similar pages](#) - [Note this](#)

PEM - Procedure **Execution** Manager

Special "**dummy**" versions of APSMpReturn and APSMpStep will be loaded from the APS Tcl/Tk .... **Synchronize** current **execution** with parallel procedure <id>. ...

[www.aps.anl.gov/asd/oag/manuals/APSPERM/APSPERM4.html](http://www.aps.anl.gov/asd/oag/manuals/APSPERM/APSPERM4.html) - 21k -

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[doc] Thread **Synchronization** Policies in DrJava

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Hence, if some **code** following a call on invokeLater depends on the **execution** of the requested action, we have a serious **synchronization** problem. ...

[www.cs.rice.edu/~javaplt/311/Readings/](http://www.cs.rice.edu/~javaplt/311/Readings/)

Revised%20Thread%20Synchronization%20Policies%20in%20DrJava.doc -

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Operating Systems Lecture Notes Lecture 3 Thread Creation ...

Nondeterministic **execution** is one of the things that makes writing parallel programs much ... Use **synchronization** operations to make **code** sequences atomic. ...

[www.cag.lcs.mit.edu/~rinard/osnotes/h3.html](http://www.cag.lcs.mit.edu/~rinard/osnotes/h3.html) - 25k -

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[PDF] FR FAMILY FR60 FAMILY ISR DOUBLE **EXECUTION**

File Format: PDF/Adobe Acrobat - [View as HTML](#)

executed. Interrupt. **sync**. Interrupt. CLKB. CLKP. EIT. Main(). ISR Code ... The RB\_SYNC macro is a simple assembler read access to a **dummy** register which is ...

[mcu.emea.fujitsu.com/.../mcu-an-300025-e-v11-fr60\\_isr\\_double\\_execution.pdf](http://mcu.emea.fujitsu.com/.../mcu-an-300025-e-v11-fr60_isr_double_execution.pdf) -

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DIGITAL Fortran 90

The -assume **dummy\_aliases** option allows **dummy** aliasing. It ensures correct results .... The other threads of the team skip the **code** and continue **execution**. ...

[www.hpc.unimelb.edu.au/doc/f90lrm/dfum\\_022.html](http://www.hpc.unimelb.edu.au/doc/f90lrm/dfum_022.html) - 31k -

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Advanced Thread **Synchronization** in Java Using Interaction Expressions  
epilog() to register that a **sync** method has finished **execution**. ... that of instance  
initializers – in interfaces by initializing a **dummy** field with the ...  
[www.springerlink.com/index/J5LFUVR RTP2A30V5.pdf](http://www.springerlink.com/index/J5LFUVR RTP2A30V5.pdf) - [Similar pages](#) - [Note this](#)

Compaq Fortran  
The default, -speculate none , means that the speculative **execution code** scheduling  
optimization ... The -assume dummy\_aliases option allows **dummy** aliasing. ...  
[www.helsinki.fi/atk/unix/dec\\_manuals/cf95au54/dfuum019.htm](http://www.helsinki.fi/atk/unix/dec_manuals/cf95au54/dfuum019.htm) - 40k -  
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Computer Languages : **Synchronization** abstraction in the BETA ...  
and that the **execution** of a specialized procedure begins in its most general part  
where the mechanics of **synchronization** can be described. ...  
[linkinghub.elsevier.com/retrieve/pii/S0096055100000047](http://linkinghub.elsevier.com/retrieve/pii/S0096055100000047) - [Similar pages](#) - [Note this](#)

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synchronize execution timing code

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### Extending Static **Synchronization** Beyond SIMD and VLIW

A more insidious VLIW constraint is, however, that the compiler must know exactly what the **execution time** will be for each region of **code**. ...

[cobweb.ecn.purdue.edu/~hankd/CARP/TREE88\\_25/paper.html](#) - 50k -

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### Waiting **Time** Analysis

For example, **execution** profiles for two **code** segments within a loop may indicate the two ... Waiting **time** can be introduced at any **synchronization** point, ...

[www.cs.rochester.edu/u/meira/spdt96/node4.html](#) - 11k -

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### Eliminating Barrier **Synchronization** for Compiler-Parallelized ...

a large percentage of total **execution time**. The compiler-generated **code** is ..... To summarize, our experiments indicate compile-time **synchronization** ...

[www.springerlink.com/index/N774VH1H715885J3.pdf](#) - [Similar pages](#) - [Note this](#)

### Apparatus and method for identification of a new secondary **code** ...

When a NEW SECONDARY **CODE EXECUTION START POINT** signal is generated in a target ... the periodic signals resulting in periodic **sync** markers in the **timing** ...

[www.patentstorm.us/patents/7225365-claims.html](#) - 19k -

[Cached](#) - [Similar pages](#) - [Note this](#)

### [PS] Reducing **Synchronization** Overhead for Compiler-Parallelized **Codes** ...

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current parallel task), comprise a large percentage of total **execution time** (14%. and 27%, respectively). The compiler-generated **code** is balanced ...

[www.kelehers.org/bibliography/doc.pl?db=papers&](#)

[table=papers&fname=han97.ps&field=ps&where...](#) - [Similar pages](#) - [Note this](#)

### Using Automatic **Synchronization**

For more information, see Synchronizing Interrupt **Code**. You can choose how the framework **synchronizes execution** of your driver's I/O request-related ...

[msdn2.microsoft.com/en-us/library/aa490059.aspx](#) - 24k -

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### Purdue's Adapter for Parallel **Execution** and Rapid **Synchronization** ...

**execution** [CoD94a] . The TTL\_PAPERS barrier mechanism also provides an effective target for compile-time instruction-level **code** scheduling [DiO92] . ...

[aggregate.org/TechPub/ICPP95/icpp95.html](#) - 55k - [Cached](#) - [Similar pages](#) - [Note this](#)

### Multi-path **synchronization** system for CNC controller - Patent 5815399

The **execution timing** for this motion command **code** is designated by the **code** Qq to be described later in detail. The **code** M9xx is a **synchronization** command ...

www.freepatentsonline.com/5815399.html - 34k - [Cached](#) - [Similar pages](#) - [Note this](#)

Multithreading Programming Topics: **Synchronization** and Locking

Semaphores offer a way to **synchronize** the **execution** of **code**. ... A critical region is a section of **code** that can be executed by only one thread at a **time**. ...

developer.apple.com/documentation/Cocoa/

Conceptual/Multithreading/articles/ThreadLocking.html - 26k -

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**time code**

to linux **time** **synchronize** ntpdate by LMZ on Jul 17, 2007. **Code execution** timer.

These two bits of **code** can be used to record & output the **execution time** of ...

snippets.dzone.com/tag/time - 43k - [Cached](#) - [Similar pages](#) - [Note this](#)

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### Long Duration Spin-wait Loops on Hyper-Threading Technology ...

One common **synchronization** technique is a long duration **spin-wait loop**. On a processor with Hyper-Threading Technology, long duration **spin-wait** loops may ...

[www.intel.com/cd/ids/developer/asmo-na/eng/20464.htm](http://www.intel.com/cd/ids/developer/asmo-na/eng/20464.htm) - 42k -

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### Evaluating Instructions Retired Events on Intel® Processors with ...

The proper parallel version of the code carefully distributes work into two equal size pieces and uses a **synchronization** variable in a "**spin-wait**" loop to ...

[www.intel.com/cd/ids/developer/asmo-na/eng/20468.htm](http://www.intel.com/cd/ids/developer/asmo-na/eng/20468.htm) - 56k -

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[More results from www.intel.com »](#)

### Re: Large (8M) cache vs. dual-core CPUs

When a **synchronization loop** needs very fast response, applications may use a **spin-wait loop**. A **spin-wait loop** is typically used when one thread needs to ...

[archives.postgresql.org/pgsql-performance/2006-04/msg00668.php](http://archives.postgresql.org/pgsql-performance/2006-04/msg00668.php) - 15k -

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### Getting ready for Hyper-Threading Technology, part 2 ...

When a thread needs to **wait** for only a brief moment to **synchronize** with another thread, it typically uses a **spin-wait loop**. "**Spin-wait**" simply indicates a ...

[www.developers.net/intelishnshowcase/view/1095](http://www.developers.net/intelishnshowcase/view/1095) - 36k -

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### Dr. Dobb's | Multithreaded Programming and Hyper-Threading ...

For **synchronization** on variables that you know are going to be imminently available, a simple **spin-wait loop** may suffice. Care is required, though, ...

[www.ddj.com/architect/184401794](http://www.ddj.com/architect/184401794) - 56k - [Cached](#) - [Similar pages](#) - [Note this](#)

### Scheduler-Conscious Synchronization

Preemption-Safe and Scheduler-Conscious Busy-Wait **Synchronization** Algorithms

.... of queue candidate->spin\_flag := failure exit loop // else need to spin ...

[www.cs.rochester.edu/research/synchronization/pseudocode/ps\\_and\\_sc.html](http://www.cs.rochester.edu/research/synchronization/pseudocode/ps_and_sc.html) - 23k -

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### A Distributed Hardware Mechanism for Process Synchronization on ...

protocol fairness, using both **spin-wait** and blocking (positive. wake-up) techniques [3]. ... **Loop synchronization** techniques have been suggested ...

[doi.ieeecomputersociety.org/10.1109/ICPP.1994.23](http://doi.ieeecomputersociety.org/10.1109/ICPP.1994.23) - [Similar pages](#) - [Note this](#)

### [PPT] Profile-guided Compiler Optimization: Loop Unrolling with Loop ...

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Global (Barrier) Event **Synchronization**. No processes can go beyond the barrier until

all processes have reached the barrier; Arrival; **Wait** for release ...  
www.cs.utexas.edu/~coonske/presentations/synchronization.ppt -  
[Similar pages](#) - [Note this](#)

Lecture notes - Chapter 13 - I/O  
This status information is used to coordinate and **SYNCHRONIZE** the useage of ...  
The little **loop** is called a **SPIN WAIT LOOP**. Something that is not well ...  
pages.cs.wisc.edu/~smoler/x86text/lect.notes/io.html - 10k -  
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mpi-1sided Mailing List Archive: Re: Volatile & Caching section  
must **synchronize** origin and target with separate MPI **synchronization** ... a window  
by local loads and remote RMA requests, a **spin-wait loop** would ...  
www.mpi-forum.org/archives/mail/mpi-1sided/0093.html - 15k -  
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S62	8	((spin\$wait) adj loop)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/22 15:03
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S65	28	((dummy) adj code) same (synchroni\$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/22 15:06
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